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EXAMINER	
STEELMAN, MARY J	

ART UNIT	PAPER NUMBER
2122	6

DATE MAILED: 06/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,098	FOEGELLE ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/3/01, 7/13/01, 5/29/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *#4, 04/03/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are pending.

Information Disclosure Statement

2. IDS received 4 March 2001 has been considered.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "30" has been used to designate both a wire and an inverter in Fig. 4. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

Fig. 2 is missing a description for #40 & #42 in the Specification.

Fig. 4 is missing a description for #36 & #38 in the Specification.

Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended.

The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1-4 recite "A translator...", should be –A translator device...-- or –A translator apparatus...-- A translator is considered a 'program per se' and is non-statutory. Examiner requests the editing of claims 1-4 to indicate an apparatus or device.

Claim 7 (l) (iii), lines 38 and 39, recites "(iii)", should be –(iv)-. This is a typo. It should be changed to refer to a 4th step. Examiner will treat this to mean "(iv)".

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 (m) (x) recites, "returning to step (m)(d)." While this is clearly a typo, Examiner cannot examine this step, as the return point is not clear. Correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

9. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being unpatentable over US Patent 5,862,354 to Curiger et al.

Per claim 1:

-a primary one-wire bus, said primary one-wire bus in digital electrical communication with the master;

(Col. 2, lines 15-17, "The present invention is a processor system that incorporates a UART adapted to operate on a one-wire bus. The UART can be master or slave device on the one-wire bus.")

-a secondary one-wire bus, said secondary one-wire bus in digital electronic communication with the one or more slave devices;

(Col. 2, lines 51-53, "The one-wire I/O circuitry can take two forms. The UART can be a master one-wire UART ("master UART") or a slave one-wire UART ("slave UART").", col. 3, lines 8-10, "A slave UART can operate on a one-wire bus with other slaves (one or more slave devices) and one master.")

-a data direction switch for directing the flow of data between said primary one-wire bus and said secondary one-wire bus.

(Col. 2, lines 56-57, "...can communicate in a bi-directional manner via an exemplary one-wire UART over a one-wire data bus.", col. 6, lines 16-17, "...status register indicates that microprocessor is to receive data from the network master..." (status register is used to indicate which direction data is to flow), col. 6, lines 9-11, "...status register...indicating that the

microprocessor wants to send data...", col. 6, lines 20-27, "...network master periodically interrogates status registers...to determine which slave UARTS have data to be transferred...")

Per claim 2:

-said secondary one-wire bus is a first secondary one-wire bus and the translator further comprises a second secondary one-wire bus.

(Col. 2, lines 64-67, "...if more than one master one-wire UART is incorporated into the same integrated circuit that each should preferably communicate on separate one-wire networks.", col. 4, lines 55-56, "...wherein each one-wire UART is connected to a separate one-wire network..." Two or more one-wire busses can exist.)

Per claim 3:

-a command parser for decoding a plurality of commands from the master.

(Col. 3, lines 13-14, "A master UART ;is the controller, hence master, of its one-wire bus. The master UART is responsible for querying the slave circuits connected to the one-wire bus", col. 3, line 45, "...master UART initiates and controls communications...", col. 4, lines 18-25, "...in the embodiment where CPU uses software and a standard port pin to emulate a master UART, the CPU must perform all of the tasks normally performed by a UART, which includes setting up appropriate bit patterns for handshaking purposes, transmitting the appropriate signals...waiting...and reading the responses...(parser decodes for a read)")

Per claim 4:

-data memory wherein data stored in said memory is output on said primary bus in response to at least one command of said plurality of commands.

(Col. 4, lines 9-11, "CPU may perform all of the processing necessary for transmitting data out of a port", col. 7, lines 21-23, "The one-wire UART of the present invention enables a microprocessor to communicate (output data) to other circuits via a one–wire bus.")

Per claim 5:

-a translator having a primary interface and a secondary interface;

(Col. 4, lines 60-66, "...a network master or master UART has the specific characteristic of being able to pull the one-wire line high...When the master circuit proceeds through its communication sequence with a slave it also initializes bus timing...", col. 5, lines 4-7, "...master UART uses the bits to specify whether electronic key, a slave , is to write a data pulse to the UART master or to read a data pulse from master..." Master UART has translator interface to send or receive data.)

-a primary one wire bus in electrical communication with said primary interface and with the master;

(Col. 4, lines 64-66, "...master circuit proceeds through its communication sequence with a slave..." Communication involves bus, interface and master.)

-a secondary one wire bus in electrical communication with said secondary interface and the slave device wherein,

(Col. 6, lines 1-4, "...a slave device can never initiate communications on its own. According to the one-wire protocol, a slave UART can only transmit and receive data upon initiation by the

network master." Communication involves bus, interface (master communication sequence) and slave device.)

-when said translator is in a first operational mode, said primary interface is in electrical communication with said secondary interface such that serial data is communicated from the master to the slave,

(Col. 5, line 7, "...read a data pulse from master ...")

-when said translator is in a second operational mode, said primary interface is in electrical communication with said secondary interface such that serial data is communicated from the slave to the master,

(Col. 5, line 6, "...write a data pulse to the UART master...", col. 6, lines 16-20, "FIG. 1 raises the voltage level to a logic 1...whenever it is writing a logic 1 to electronic key (slave) or whenever it expects electronic key to write to the master UART...")

-when said translator is in a third operational mode, serial data is not communicated between the master and the slave.

(Col. 5, lines 30-32, "A situation in which network master does not attempt to raise the voltage level ...is when it is writing logic 0 to the slave.")

10. Claims 6 & 7 are rejected under 35 U.S.C. 102(b) as being unpatentable over US Patent 6,412,072 B2 to Little et al.

Per claim 6:

A method (col. 2, lines 49-50) for inserting known data into a serial data stream between a master and a slave device on a one-wire bus including the steps of:

(a) providing a translator having a primary one-wire bus in electrical communication with the master and a secondary one-wire bus in electrical communication with the slave device, said translator providing interruptible communication between the master and the slave device;
(Col. 12, lines 62-63, "...vector the microcomputer to the assigned interrupt routine..." (translator redirects execution), col. 26, lines 58-61, "In the case of testability, the electronic module has been designed to support an external high speed interface for use at wafer level probe tests.", col. 35, line 27-col. 36, line 4, "Probe Evaluation...The source of the code is supplied through either the external emulation bus...or from the internal SRAM...Final Test Evaluation: The Final Test Evaluation is totally controlled through the One Wire UART...microcomputer will...run from a special test ROM...Emulation:...will access external memory using the emulation bus..." A testing and emulation feature is disclosed. An interrupt can send execution to an external memory.)

(b) decoding a set of commands sent by the master on the primary one-wire bus;
(Col. 5, line 67 – col. 6, line 5, "The peripheral circuits decode the address and, if appropriate, will combine the address with additional control signals from the microprocessor core so that the peripheral blocks understand what to do...will either read or write from the databus."

(c) in response to one or more commands of said set of command, interrupting communication between the master and the slave device;

(Col. 12, line 58, "One Wire Slave UART Interrupt Command:...interrupt is designed to both restart...and to also vector...to the assigned interrupt routine...")

(d) sending known serial data to either the master or the slave device.

(Col. 12, lines 10-18, "Interrupt Logic: designed to allow...the One Wire Interrupt command...", col. 26, lines 58-61, "Testability...support an external high speed interface...", col. 35, line 25-col. 36, line 4, "The initial Test Probe Evaluation makes use of two different teat modes...electronic module can be configured to provide one of four different memory maps to access and test all of the memory blocks and internal core logic...The source of the code is supplied through either the external emulation bus of from the internal SRAM..." An interrupt can be used to vector to a known test data.)

Per claim 7:

A method (col. 2, lines 49-50) for inserting known data into a data stream between a master and a slave device on a one-wire bus including the steps of:

(Col. 3, lines 1-2, "FIGS. 71, 7B, 7C, and 7D depict a flow chart indicating an exemplary operation of the one wire UART", col. 19, lines 54-55, "The protocol required for the UART memory function commands is depicted in FIGS. 7A through 7D, col. 35, line 25- col. 36, line 4 provides a discussion on testing and emulation abilities of the invention.

(a) providing a primary one-wire bus in electrical communication with the master;

(Col. 2, lines 21-26, "...comprises a one wire (single wire) interface for bidirectionally interfacing the electronic module with another electronic device. The one wire interface is connected to a one wire UART. The UART is connected to a microprocessor and a co-processor and a memory circuit", col. 5, lines 18-20, "...microprocessor core block communicates with other circuitry blocks via a control databus. The databus in the preferred embodiment is a standard 8051 interface bus...")

(b) providing a secondary one-wire bus in electrical communication with the slave;

(Col. 7, lines 65-67, "It is understood that the present invention is not limited to a single wire connection between a master/host and the electronic module.", col. 8, lines 9-16, "FIG. R is a slave one wire UART block diagram...One is the one wire front end which connects to the OWSE pad (one wire slave UART). The other part of the slave one wire UART block diagram is a memory area with control logic called the data read write area. The one wire front end provides standard routine protocols used in one wire communications.", See FIG. 4)

(c) waiting for a reset pulse on said primary one-wire bus;

(See FIGs. 7 A-D, "Reset" at the bottom of the drawings.)

(d) receiving a ROM command on said primary one-wire bus;

(See FIGs. 6A & 7A, "From ROM functions flowchart, at the top of the drawings.)

(e) determining if said ROM command is a read command, a match command, a search command, or a skip command;

(See FIGs. 6A & 6B, note 1/3 of way down chart a selection is made between the ROM functions. Col. 19, lines 21-27, "The One Wire front end is access via a single data line using the One Wire Protocol. The bus master must provide one of the seven ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Alarm Search, 5) Skip ROM...")

(f) if said ROM command is a read command, performing the steps of:

(i) transmitting a predetermined identifier on said primary one-wire bus;

(ii) returning to step (c)

(See FIG. 6A, note selection for "Read Command" on the left., col. 19, lines 19-21, "The bus master must provide one of the seven ROM Function Commands...")

(g) if said ROM command is a match command performing the steps of:

(i) receiving an identifier on said one-wire bus;

(ii) comparing said received identifier to a predetermined identifier;

(iii) proceeding to step (j)

(See FIG. 6A, note the selection for the "Match ROM" command and the following bit match (comparing identifier).)

(h) if said ROM command is a search command performing the steps of:

(i) transmitting the first bit of a predetermined identifier having a plurality of bits on said primary one-wire bus;

(ii) transmitting the complement of said first bit of said predetermined identifier on said primary one-wire bus;

(iii) receiving a bit on said primary one-wire bus;

(iv) comparing said received bit to said first bit of said predetermined identifier;

(v) repeating steps (h)(i) through (h)(iv) for each bit of said plurality of bits;

(vi) proceeding to step (j);

(See FIG. 6A, note the selection for the "Search ROM" command, transmitting bits, transmitting the complement , receiving, comparing for each bit.)

(i) if said ROM command is a skip command proceeding to step (j);

(See FIG. 6A, note the "Skip ROM" command selection.)

(j) receiving a memory command from said primary one-wire bus;

(See FIG.7A, Memory Functions Flow Chart, top left .)

(k) receiving a memory address from said primary one-wire bus;

(See FIG.7A.)

(l) if said memory command is a read command performing the steps of:

(i) receiving slave data on said secondary one-wire bus;

(ii) transmitting said slave data on said primary one-wire bus;

(iii) repeating steps (l)(i) – (l) (ii) until a reset pulse is received on said primary one-wire bus;

(iv) returning to step (d);

(See FIG.7A, "Slave One Wire Memory Function Flow Chart", note "Read Status" on the left, processing through reset.)

(m) if said memory command is a write command, performing the steps of:

(i) receiving slave data on said primary one-wire bus;

(ii) transmitting said slave data on said secondary one-wire bus;

(iii) receiving verification data on said secondary one-wire bus;

(iv) transmitting said verification data on said primary one-wire bus;

(v) receiving a write pulse on said primary one-wire bus;

(vi) transmitting a write pulse on said secondary one-wire bus;

(vii) receiving said slave data on said secondary one-wire bus;

(viii) transmitting said slave data on said primary one-wire bus;

(ix) repeating steps (m)(i) – (m) (viii) until a reset pulse is received on said primary one-wire bus;

(See FIG.7A, "Slave One Wire Memory Function Flow Chart", note "Write Status" , CRC correct (verification data), processing through reset.)

(x) returning to step (m)(d).

(This feature is not examined. See comments under the 112 35 USC rejection above.)

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (703) 305-4564. The examiner can normally be reached Monday through Thursday, from 7:00 A.M. to 5:30 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552.

The fax phone number is (703) 872-9306 for regular communications and for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Mary Steelman

06/09/2004

TUAN DAM
SUPERVISORY PATENT EXAMINER